COMSAT LABORATORIES' ON-BOARD BASEBAND SWITCH DEVELOPMENT*

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SUMMARY

Work performed at COMSAT Laboratories to develop a prototype on-board baseband switch is summarized. The switch design is modular to accommodate different service types, and the architecture features a high-speed optical ring operating at 1 Gbit/s to route input (up-link) channels to output (down-link) channels. The switch is inherently a packet switch, but can process either circuit-switched or packet-switched traffic. If the traffic arrives at the satellite in a circuit-switched mode, the input processor packetizes it and passes it on to the switch. The main advantage of the packet approach lies in its simplified control structure. Details of the switch architecture and design, and the status of its implementation, are presented.

INTRODUCTION

It is likely that future generations of satellites will incorporate increased use of multiple spot beams. This will lead to increased spacecraft antenna gains, resulting in higher down-link power densities and increased satellite gain-to-noise temperature ratio (G/T). Both of these factors facilitate the use of smaller and lower cost earth stations.

The increased use of multiple spot beams will require additional switching on board the satellite in order to connect up-link beams to down-link beams. This switching can be accomplished either statically or dynamically. When the number of beams is large, static switching becomes impractical and dynamic switching is needed. This can be performed either at RF or IF using a microwave switch matrix (MSM), or at baseband with a baseband switch. The use of MSMs is almost exclusively limited to high-speed time-division multiple access (TDMA) systems, since switching is performed across an entire transponder. Baseband switching is suited for either TDMA or frequency-division multiple access (FDMA) operating in either a continuous or burst mode. Baseband switching may also be coupled with other forms of on-board processing, such as on-board regeneration, decoding and recoding, and

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demultiplexing and remultiplexing. These additional features can lead to improved performance, greater flexibility, and less complex earth station design.

SWITCH ARCHITECTURE

The baseband switch under development at COMSAT Laboratories is intended to provide switching between six input ports and six output ports. Each port will accommodate bit rates of up to 120 Mbit/s (extendable to 155 Mbit/s). Figure 1 shows the modular structure of the baseband switch, which provides for both interbeam connectivity (input ports switched to output ports) and interservice connectivity (i.e. connectivity between TDMA and FDMA services). This is accomplished within the input and output (service-dependent) modules, as shown in Figure 1. Any mix of FDMA and TDMA inputs or outputs may be accommodated by the baseband switch. Interconnectivity between service types can lead to simplification in the ground segment, since any earth station can employ a single transmission method that is optimized for its own service requirements rather than those of its correspondents.

A number of switch architectures were examined for possible implementation (see Figure 2). These included the conventional space switch and a time switch. It was assumed that either switch would process traffic data on a frame by frame basis (typically 2ms). For the space switch, all input modules transmit simultaneouly; therefore, the physical paths within the switch must be changed to route traffic data from a given input module to each output module. This requires that the switch never simultaneously connect two input modules to the same output module. In contrast, the time switch works by having each input module transmit in a time-division multiplexed (TDM) sequence. Traffic data sent by a given transmitting module are received by all output modules, on either a bus or ring. Only traffic data intended for a given output module are retained by that module. Since the time switch shares (in time) the interconnection medium, the physical connection does not change. For this reason, control of the time switch was considered to be less complex than that of the space switch.

The aggregate information bit rate of the switch is 6 x 120 Mbit/s, or 720 Mbit/s. To allow for TDM guard times and overhead inefficiencies, a switch speed of about 1 Gbit/s (960 Mbit/s) was selected. Mass, power, size, and radio frequency interference (RFI) considerations led to the selection of an optical implementation.

Bus and ring switch topologies were considered for the switch implementation. The selected topology is shown in Figure 3. The traffic data are routed on a high-speed fiber optic ring. The ring topology was selected over the bus topology for traffic routing because the hardware for the input and output modules is less complex. Specifically, the modules in a ring topology process continuous data, while in the bus topology they process burst data. Because of this, data synchronization is less complex for the ring topology, leading to a design with lower power dissipation.

The clock that provides timing is distributed to each module via a fiber optic star network. Bus, ring, and star topologies were examined for this function, and the star topology was found to consume the lowest power considering the combined power of the diode lasers and photodetectors needed for implementation.

The switch operates with a 2-ms TDM frame, as depicted in Figure 3. The configuration processor starts each frame by placing a frame marker and its control information onto the optical ring. Input module 1 is the first module to receive the frame marker and control information. It reads the control information intended for it, appends its traffic data and status information to the configuration processor data, and sends the combined data on to input module 2. Input modules 2 through 6 each read the control data in turn and append their traffic data and status information to the data currently in the frame. Subsequently, each output module reads the traffic data intended for it, appends its status information to the received data, and sends the combined data on to the next module. Output module 6 sends the complete frame to the configuration processor, which reads the status information from each module. The process is repeated for the next TDM frame by the configuration processor placing the frame marker and its control information onto the optical ring.

Figure 3 also shows the static bypass switches which enable a failed module to be taken off line. Redundancy may be provided by using n-for-m modules, with n - m modules in the bypass mode.

Traffic data are routed through the switch using a packet-switched approach. For traffic that reaches the satellite in a circuit-switched manner, the input modules packetize the channels into cells containing eight channels. Each cell contains traffic data for the same output module or modules (for multicast) and is labeled with a destination header in its routing field. The control information from the control processor provides the routing and configuration information to the input modules for cell generation. The routing data provided by the control processor for each input module comprises the routing maps of input channels to output modules on a frame-by-frame basis. In addition, for FDMA transmissions, configuration information is provided that maps up-link carriers to input modules and output modules to down-link carriers. This information changes very infrequently, only when carrier frequency plans are changed.

If the traffic data arrive at the satellite in a packet-switched format, the control processor will only provide framing information, since the routing control is contained within the packet headers. This is the most effective method for operating the switch and results in the least complex on-board hardware; however it does require that the earth stations packetize the traffic data with routing headers.

The format for the packet data that flow in the optical ring is shown in Figure 4. The 2-ms frame is partitioned into 1,667 time slots, each capable of transferring a single cell (data unit) between modules. Each cell contains 9 x 128 data bits. The first 128 bits are the cell header, and the remaining 8 x 128 bits correspond to eight 64-kbit/s traffic channels.

SWITCH DESIGN

The switch, shown in Figure 5, employs a modular design which partitions the core switching functions from the service-dependent functions. The design and implementation effort to date has concentrated on the core switching modules.

Semicustom implementations using standard cell or gate array technologies are being targeted to minimize the size and power requirements of the switch. Each module will require about 20 to 30 chips and will be implemented on a 5 x 5-inch (approximately) circuit board. The core switch module (Figure 6) incorporates two application-specific intergrated circuits (ASICs). Chip 1 is the high-speed switch interface ASIC, and chip 2 is the switch core processor ASIC. This design will permit a module to serve as either an input or output module.

The high-speed switch interface ASIC interfaces at 960 Mbit/s to the optical fiber ring. This is accomplished with one diode laser transmitter on the transmit side for the traffic and status data, and two photodetectors on the receive side, one for data and one for clock. The diode laser used in the design draws 720 mW of power and produces about 1 mW of optical power. The efficiency of these devices is expected to increase significantly in the next few years. This chip accepts the optical clock and optical traffic and control data from the ring and transfers traffic and status data to the ring. To perform these functions, the ASIC establishes and maintains frame synchronization, phase-aligns the clock and data, encodes/decodes packet headers, and interfaces to the switch core processor and data random-access memory (RAM) over the 16-bit traffic data bus.

Because of the speed required, the high-speed switch interface ASIC uses a gallium arsenide (GaAs) technology. It is estimated that this chip will require 6,000 gates and have a total pin count of 84. The estimated power dissipation for the chip is slightly less than 2 W.

The switch core processor ASIC transfers data between the service-dependent module and the core processor module. For circuit-switched traffic, it accepts and executes configuration and routing commands from the configuration processor. The configuration information is sent to the output modules as part of the routing header to identify the appropriate down-link carrier for FDMA transmissions. This chip sorts and routes both the circuit- and packet-switched data to the appropriate output module. For circuit-switched traffic, the switch core processor ASIC in an input module sorts and packetizes the traffic into cells containing eight 64-kbit/s channels to the same destination(s), attaches a routing header, and sends the packet to the RAM for transfer to the high-speed switch interface ASIC. For packet-switched traffic, this step is eliminated. When used in an output module, this chip routes incoming packet data to the appropriate down-link carrier.

The device for the switch core processor will likely be implemented in complementary metal-oxide semiconductor (CMOS) technology having an estimated gate count of 50,000 with a pin count in the range of 256 to 312. The estimated power dissipation for this chip is 2.6 W. Table I gives an estimated breakdown of the power dissipation for the core module.

TABLE I

Core Module	Power Dissipation (W)
HSSI ASIC	1.9
SCP ASIC	2.6
RAM	1.7
Diode Laser (1)	0.7
Photodetector (2 @ 0.6 W)	1.2
Total	8.1

The physical layout of the baseband switch is given in Figure 7. The input and output modules will be housed in two separate sets of trays, each containing one core module and one service-dependent module. This packaging approach permits the input modules to be physically separated from the output modules. Within a spacecraft, for example, it will be possible to locate the input modules close to the receivers and the output modules close to the high-power transmitters. For the distances required, the loss in the fiber optic ring is neglegible. In addition, RFI to or from the optical fiber is nonexistant.

A breadboard circuit (Figure 8) of the critical functions of the switch has been built and tested. The critical functions include the phase adjustment circuit, which aligns the clock and data; integration of the optical to electrical and electrical to optical converters; and fabrication at Gbit/s speeds using surface-mount devices. The phase adjustment breadboard circuitry, using a broadcast clock and ring data, was successfully built and tested using surface-mount devices. The conversion of 1-GBit/s data from electrical to optical and back to electrical was also successfully demonstrated on the breadboard.

CONCLUSIONS

Work continues at COMSAT Laboratories on development of the high-speed on-board baseband switch. The design of the configuration processor module and the high-speed switch interface ASIC is complete. It is expected that the ASIC will be fabricated and tested before the end of 1991. The core processor ASIC design is about 75 percent complete and it is expected that this chip will be fabricated in early 1992. Testing of the core switching functions is expected to begin by mid-1992. The design of the service-dependent functions is expected to be completed by the end of 1992. The complete switch, including the service-dependent modules, will be tested in 1993.

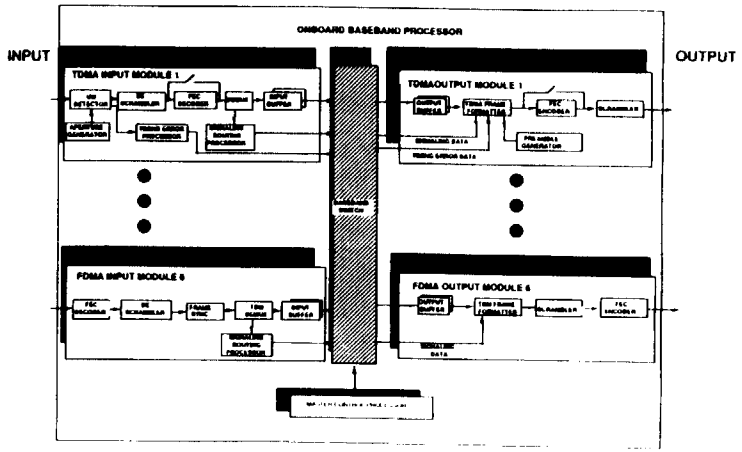

Figure 1: Onboard Baseband Switch

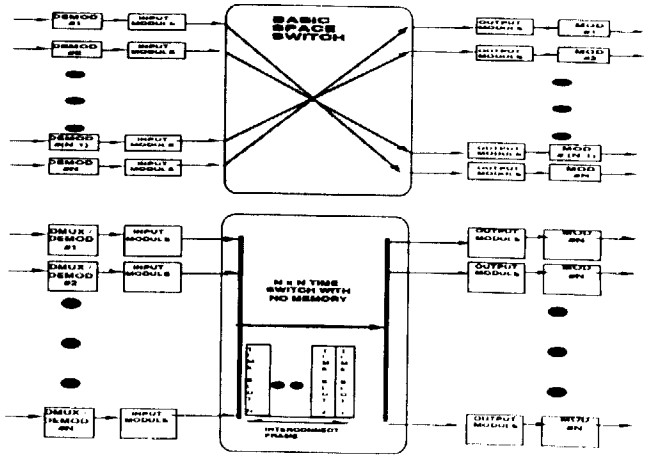

FIGURE 2: EXAMPLE OF TIME & SPACE SWITCH

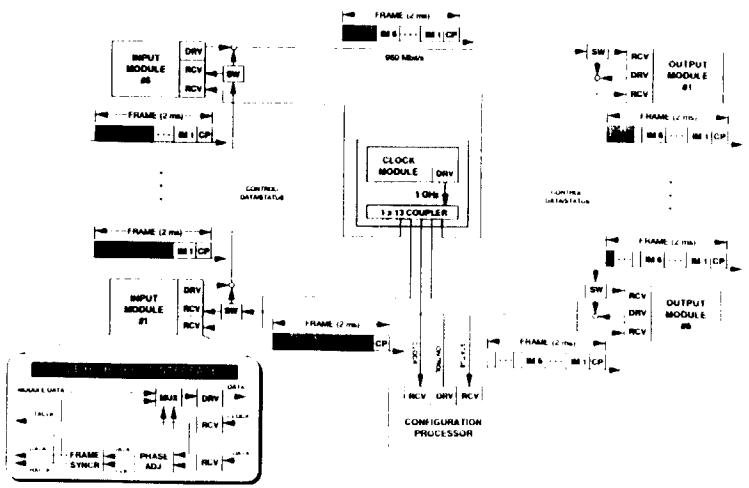

Figure 3: 1-Gbit/s ON-BOARD BASEBAND SWITCH ARCHITECTURE

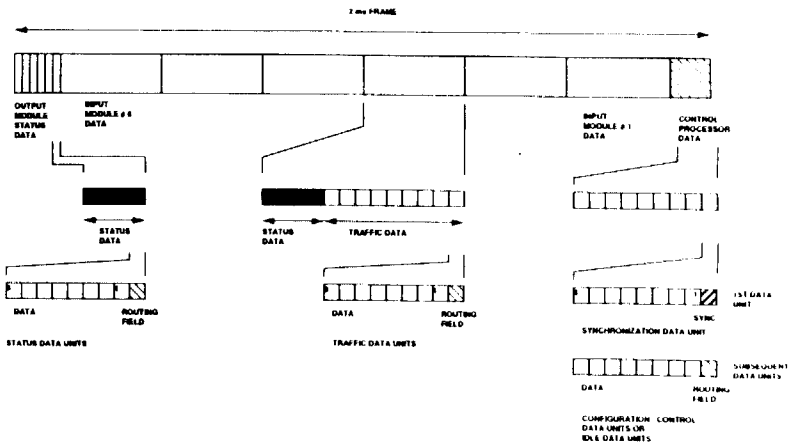

Figure 4: Frame Format

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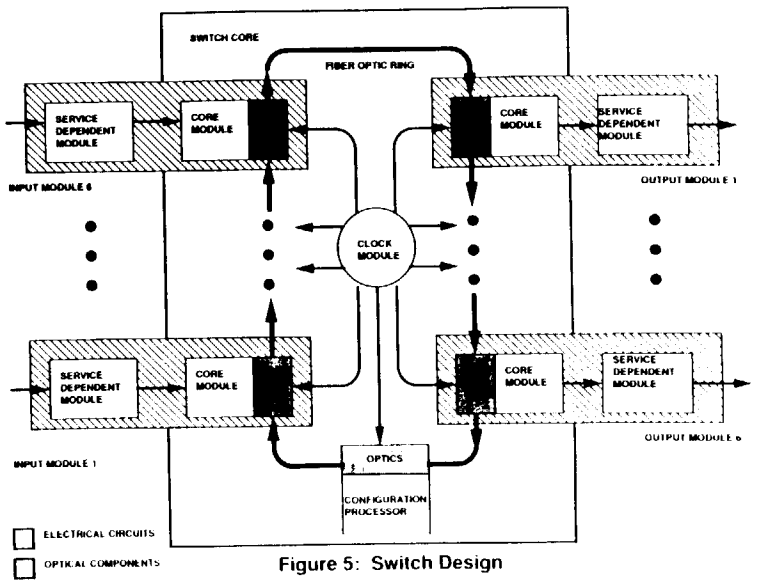

Figure 5: Switch Design

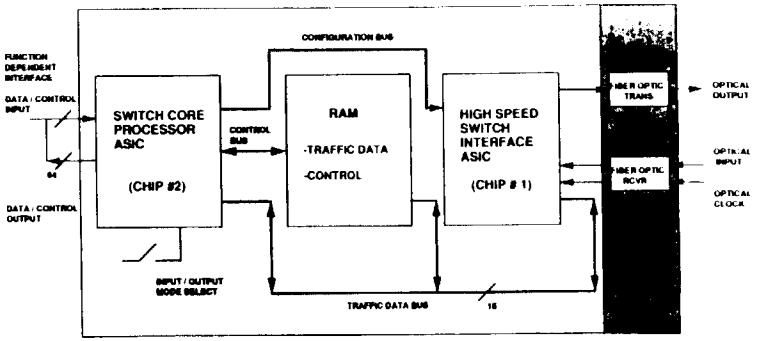

FIGURE 6: Core Module Design

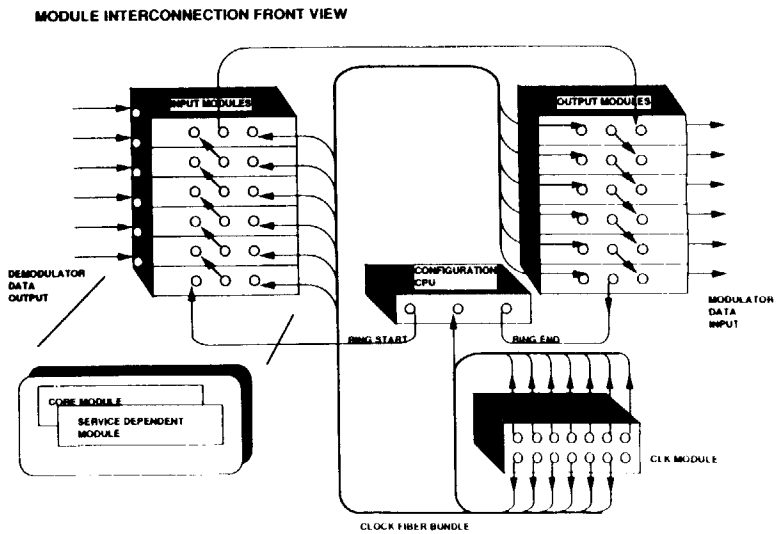

FIGURE 7: Physical Layout of Switch

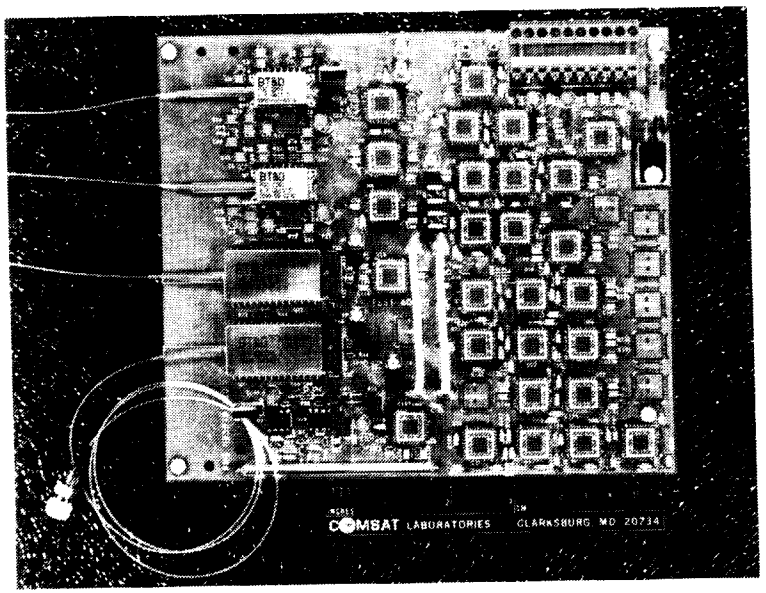

Figure 8: Breadboard Circuit